reduced. This practice produces inaccurate results in the reading circuits since they are also driven by V_{CC}.

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In the present invention, the variability of V_{CG} independent of voltages supplied to the reading circuit produce more accurate and reliable results.

Furthermore, the wide range of V_{CG} is useful during testing and diagnostic of the EEprom. It allows the full range of the programmed cell's threshold to be measured easily by continuing to increase V_{CG} (up to the maximum limited by the device's junction breakdown).--

IN THE DRAWINGS:

N.E.

Add the accompanying sheets 6-22 of drawings, in informal form, which contain additional Figures 9-27.

IN THE CLAIMS:

Please cancel the original parent application claims 1-62, without prejudice, and substitute the following new claims therefore:

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--63. A non-volatile memory system provided on a single integrated circuit chip for storing inputted data therein, comprising:

an array of electrically alterable memory cells that individually include a field effect transistor having a storage element and a threshold level that is variable in accordance with an amount of charge carried by the storage element, said array being divided into blocks of cells that are resettable together, cells within said blocks being addressable for application of programming voltage conditions to individually program them into one of more than two distinct threshold level ranges corresponding to more than one bit of input data per cell,

a reset circuit that simultaneously applies reset voltage conditions to the cells within individual blocks to drive the effective threshold levels of such cells to a reset state,

a programming circuit that applies the programming voltage conditions in parallel to a plurality of addressed cells within a reset block to drive the effective threshold voltage of the addressed cells toward one of the more than two programmable threshold level ranges in accordance with a chunk of inputted data being stored therein,

a reading circuit that monitors in parallel the threshold level ranges of the plurality of addressed cells, and

a control circuit that individually terminates application of the programming voltage conditions to any one of the plurality of addressed cells when the reading circuit verifies that said any one cell has reached the programmable threshold level range that

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corresponds to the inputted data being stored therein, while enabling further application of the programming voltage conditions to others of the plurality of addressed cells that have not yet been so verified, until all of the plurality of addressed cells are verified to have correctly been programmed with the chunk of inputted data.

64. The memory system according to claim 63, wherein the plurality of addressed cells are less than a number of cells within the individual blocks.

65. The memory system according to claim 63, wherein the control circuit includes a plurality of latches and means for setting individual ones of the latches in response to corresponding ones of said plurality of addressed cells being verified.

66. The memory system according to claim 63, wherein said more than two distinct threshold level ranges are non-overlapping and separated from each other by two or more breakpoint threshold levels.

67. The memory system according to claim 66, wherein the reading circuit includes means for ascertaining the individual threshold level ranges of the plurality of memory cells after the cells have been programmed into the individual threshold level ranges beyond one of their breakpoints by a margin.

68. The memory system according to claim 63, wherein the programming circuit causes the plurality of addressed cells to be programmed with successive applications of said programming voltage conditions, and the reading circuit operates to monitor the threshold level ranges of the plurality of addressed cells in between applications of said programming voltage conditions.

69. The memory system according to claim 68, wherein the programming circuit further shifts the threshold levels of the individual addressed cells by less than one half of a difference between at least two breakpoint threshold levels defining one of the threshold level ranges.

70. The memory system according to claim 68, wherein the programming circuit further operates with programming voltage conditions that requires a plurality of said successive applications of programming voltage conditions in order to change individual ones of the plurality of addressed cells from one of the threshold level ranges to another adjacent threshold level range.

71. The memory system according to claim 63, wherein the control circuit includes a comparator receiving the monitored threshold level range of the plurality of addressed cells and the input data being programmed into the plurality of addressed cells for

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verifying when the individual ones of the plurality of cells reach the programmable threshold level that corresponds to the inputted data being stored therein.

72. The memory system according to claim 63, wherein at least one reference cell is included in individual ones of the blocks of cells, and which additionally comprises means for programming said at least one reference cell to a reference level, and wherein said reading circuit includes means for reading the reference level of the reference cell of the block wherein the plurality of addressed cells exists to verify that any one cell has reached a desired one of the more than two distinct threshold level ranges.

73. The memory system according to claim 63, wherein the reset circuit includes means operable after application of the reset voltage conditions to an addressed at least one block for adjusting to the reset state any cells of said at least one block that were over erased by the reset voltage condition application.

74. The memory system according to claim 63, wherein the reset circuit includes means for selecting one or more of the blocks to be reset, and means responsive to the selection means for simultaneously applying the reset voltage condition to the memory cells within all of the selected blocks.

75. The memory system according to claim 74, wherein the block selecting means includes a register associated with individual ones of the blocks for containing an indication whether the associated block is to be erased.

76. A non-volatile memory system provided on a single integrated circuit chip for storing inputted data therein, comprising:

an array of electrically alterable memory cells that individually include a field effect transistor having a storage element and a threshold level that is variable in accordance with an amount of charge carried by the storage element, said array being divided into blocks of cells that are resettable together,

a reset circuit that simultaneously applies reset voltage conditions to the cells within individual blocks to drive the effective threshold levels of such cells to a reset state,

a programming circuit that applies the programming voltage conditions in parallel to a plurality of addressed cells within a reset block,

a reading circuit that verifies in parallel the state into which the addressed plurality of cells are programmed,

means for inhibiting further programming of correctly verified cells among the plurality of addressed cells, and

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means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

77. The memory system according to claim 76, wherein cells within said blocks are addressable for application of programming voltage conditions to individually program them into one of more than two distinct threshold level ranges corresponding to more than one bit of input data per cell, and wherein the programming circuit operates to drive the effective threshold voltage of the addressed cells toward one of the more than two programmable threshold level ranges.

78. The memory system according to claim 77, wherein said more than two distinct threshold level ranges are non-overlapping and separated from each other by two or more breakpoint threshold levels.

79. The memory system according to claim 76, wherein the programming circuit causes the plurality of addressed cells to be programmed with successive applications of said programming voltage conditions, and the reading circuit operates to monitor the threshold level ranges of the plurality of addressed cells in between applications of said programming voltage conditions.

80. The memory system according to claim 76, wherein at least one reference cell is included in individual ones of the blocks of cells, and which additionally comprises means for programming said at least one reference cell to a reference level, and wherein said reading circuit includes means for reading the reference level of the reference cell of the block wherein the plurality of addressed cells exists to verify that any one cell has reached the desired threshold level range.

81. In a data storage system having an array of memory cells that individually include an element that stores an electrical charge level that is alterable in response to appropriate voltage conditions being applied to the cell in order to set a variable threshold level thereof into a range that is determinable by reading the cell, the array being organized into blocks of cells that are electrically resetable together to a common threshold level, a method of operation, comprising:

simultaneously electrically resetting a number of said blocks less than all of the blocks in the array,

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applying said appropriate voltage conditions in parallel to a plurality of said memory cells within one of the reset blocks in accordance with a chunk of user data, thereby to alter the charge levels on the storage elements of said plurality of memory cells,

determining the threshold level ranges in which individual ones of said plurality of memory cells lie, and

terminating the application of appropriate voltage conditions to individual ones of said plurality of memory cells upon their being determined to have reached desired threshold level ranges while continuing to apply said appropriate voltage conditions to others of said plurality of cells until all of the plurality of cells are determined to have reached their desired threshold level ranges corresponding to said chunk of user data.

82. The method of claim 81, wherein there are exactly two threshold level ranges.

83. The method of claim 81, wherein there are more than two threshold level ranges.

84. The method of claim 81, wherein the threshold level ranges are separated by exactly one breakpoint threshold level, thereby to provide exactly two non-overlapping threshold level ranges.

85. The method of claim 81, wherein the threshold level ranges are separated by more than one breakpoint threshold level, thereby to provide more than two non-overlapping threshold level ranges.

86. The method of claim 81, additionally comprising, after all of the plurality of cells are determined to have reached their desired threshold level ranges corresponding to said chunk of user data, repeating the applying, determining and terminating operations to additional pluralities of cells within the reset block in order to store additional chunks of user data within the reset block.

87. The method of claim 81, wherein individual ones of the blocks of cells contain a number of spare cells, and further wherein the spare cells within a particular block are substituted in place of any defective cells within said plurality of cells of said particular block.

88. The method of claim 81, wherein the plurality of cells are determined to have reached the desired threshold level ranges by comparing the threshold levels of the plurality of cells with the chunk of user data.

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